IN THE CLAIMS

Please cancel claims 15 and 16 without prejudice.

Please amend claims 1-2, 4-9, 13-14, and 17-21 as indicated below.

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1. (Currently Amended) A method comprising:

enabling a special programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for internal program verification and wherein [[the]] enabling special programming mode disables the internal program verification by the automation circuitry of the memory;

programming a plurality of words into the memory during the special programming mode without having the automation circuitry of the memory ~~performing~~ to perform the internal program verification; and

exiting the special programming mode of the memory after the plurality of words have been programmed into the memory.

2. (Currently Amended) The method of claim 1, further comprising verifying the plurality of words programmed into the memory by a processor other than the memory ~~with a verification processor by resending the plurality of words previously sent into the memory~~.

3. (Original) The method of claim 2, wherein the verification ~~processor~~ is performed by an external host processor.

4. (Currently Amended) The method of claim 2, further comprising enabling internal program verification by the memory after exiting the special programming mode ~~and wherein the verification processor is the memory an internal program verification processor of the memory~~.

5. (Currently amended) The method of claim 2, wherein the verifying further includes:

determining if all of the words in the plurality of words are verified;

if any one of the plurality of words does not verify, then repeating the programming of the entire plurality of words and repeating the verification by the processor other than the memory; and

if all of the plurality of words verify, then exiting the special programming mode of the memory.

6. (Currently amended) The method of claim 2, wherein the verifying further includes:

determining if all of the words in the plurality of words are verified;

if any one of the plurality of words does not verify, then repeating the programming of the [[one]] word that did not verify and repeating the verification by the processor other than the memory; and

if all of the plurality of words verify, then exiting the special programming mode of the memory.

7. (Currently Amended) The method of claim 1, wherein upon exiting the special programming mode of the memory, the special programming ~~user interface~~ mode is permanently disabled.

8. (Currently Amended) The method of claim 1, wherein upon exiting the special programming mode of [[the]] memory, the internal program verification by [[the]] memory is enabled.

9. (Currently Amended) The method of claim 1, wherein the programming of the plurality of words into the memory comprises using only a single programming pulse for each bit of each word of the plurality of words.

10. (Previously presented) The method of claim 1, wherein the programming of the plurality of words into the memory without the memory performing internal program verification continues until a programming ending condition is met.

11. (Original) The method of claim 10, wherein the programming ending condition is a pre-selected time.

12. (Original) The method of claim 10, wherein the programming ending condition is an ending address.

13. (Currently Amended) An apparatus comprising:

a memory comprising:

an automation circuitry to perform internal program verification unless the automation circuitry is disabled;

a special programming mode circuitry to disable ~~the internal program verification by~~ the automation circuitry that performs the internal program verification when the special programming mode circuitry is enabled; and

a host processor communicatively coupled to the memory, the host processor ~~including:~~

~~a circuit to send~~ sending to the memory a plurality of words to be programmed into the memory without the memory performing the internal program verification during the special programming mode; and

~~a circuit to exit~~ exiting the special programming mode of the memory after the plurality of words have been programmed into the memory.

14. (Currently Amended) The apparatus of claim 13, wherein the host processor further ~~includes a circuit to verify~~ verifies the plurality of words programmed into the memory without having the memory to perform the internal verification.

15. – 16. (Canceled)

17. (Currently Amended) The apparatus of claim 14, wherein the ~~circuit to verify includes:~~ the host processor, without invoking the internal program verification of the memory,

~~circuitry to determine if all of the words in the plurality of words are verified; and~~

reads back from the memory the words that have been programmed into the memory, and

~~circuitry to compare~~ compares the plurality of words stored in a second memory coupled to the host processor with a plurality of words read back from the memory to verify whether the words have been programmed into the memory successfully ~~by the host processor~~.

18. (Currently Amended) The apparatus of claim 17, wherein the host processor further ~~comprises: a circuit to reprogram~~ reprograms the entire plurality of words if any one of the plurality of words is not verified successfully by the host processor ~~does not verify~~.

19. (Currently amended) The apparatus of claim 17, wherein the host processor further ~~comprises: a circuit to reprogram~~ reprograms one or more words that ~~are not verified~~ did not verify successfully.

20. (Currently amended) The apparatus of claim 13, wherein the ~~circuit to exit the special programming mode of the memory~~ the host processor disables the special programming mode circuitry when exiting the special program mode of the memory.

21. (Currently Amended) The apparatus of claim 13, wherein the ~~circuit to exit the special programming mode of the memory~~ host processor enables the internal program verification performed by the memory.

22. (Original) The apparatus of claim 13, wherein the special programming mode circuitry is disabled when a programming ending condition is met.

23. (Original) The apparatus of claim 22, wherein the programming ending condition is a pre-selected time.

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24. (Original) The apparatus of claim 22, wherein the programming ending condition is an ending address.